Adarate Systems

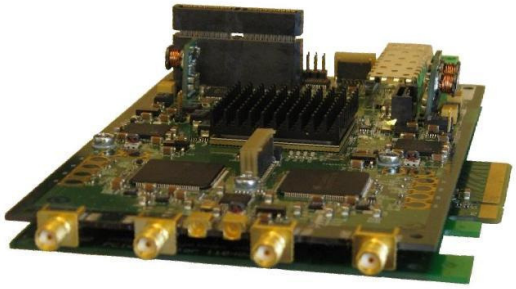
TECH BRIEF

Feb 2012

*d*HRFT

High-Speed Radio Frequency Transceiver

The *d*HRFT board is a dual channel HRFT version and features dual Gigasample Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs) tightly coupled to a Virtex-6 FPGA. The board can stream two channels of RF-data (baseband) with a sampling frequency up to 3 Gsps (recording) and 2,5 Gsps (transmitting). The analog input bandwidth is 3 GHz, which makes it suitable for subsampling applications. For communication of measurement data from the board and for example RF waveforms to the board, the board is equipped with two SFP cages. Those support optical or copper connectivity such as GbE, SONET/SDH etc with rates up to 3,125 Gbps. The GbE links are also used to control the board.



FEATURES

- Two 8-bit 3 Gsps low power ADCs.
- Two 14-bit 2,5 Gsps low power DACs.
- One Virtex-6 FPGA.
- Two GbE, serial port and USB connectivity.
- Digital High-Speed connector for stacking supporting multiple Gbit LVDS pairs.
- GTX connectivity, 8 x 6,6 Gbps/lane.
- Supervision of temperature and power.
- Single 12V DC supply.
- Eurocard form factor (100x160 mm).

OPTIONAL

- Connectivity possible with 2 x 10 GbE, via expansion socket.
- FLASH memory on board.
- FPGA up to XC6VSX475T (the FF1156 package).
- GPS connection.
- Flexible analog front-end interface.
- Disc Storage 2+ GByte/s (via PCIe).
- Sample Data Memory.
- SATA (3rd party IP).
- PCIe via adapter board up to x8 Gen 2 (GTX).
- Industrial temperature grade.

OTHER HRFT

- *i*HRFT – *the one channel version*
  Interleaved ADC's and a single 6 Gsps DAC gives a one-channel-solution up to 6 Gsps.
- *q*HRFT – *the quad channel version*
  A quad ADC channel solution with two DAC channels. Each ADC channel runs at maximum 1,5 Gsps and the two DACs at 2,5 Gsps.
- *f*HRFT – *the FMC version*
  Via the FMC connector on board a flexible use of different front-ends is provided.

FUTURE HRFT

- *i2*HRFT – *2nd gen ONE-channel board with* ADC front-end up to 8+ Gsps.
- *d2*HRFT – *2nd gen DUAL-channel board with* 10- or 12-bit dual ADC front-end up to 4+ Gsps per channel.
- *q2*HRFT – *2nd gen QUAD-channel board with* 10- or 12-bit quad ADC front-end up to 2+ Gsps per channel.

Analog in
Two 8-bit 3 Gsps ADC (ADC083000 from National Semiconductor)

Specification: ENOB ~ 7 bits and SNR ~ 44,5 dB. The two inputs are single-ended through SMA or differential through SMP connectors.

Analog out
Two 14-bit 2,5 Gsps DAC (AD9739 from Analog Devices)

Specifications: SFDR ~ 69,5 dBc at f_{out} ~ 100 MHz and 2,4 Gsps. Supports three Nyquist zones also using F_s mixed mode or Return-to-Zero mode. The two outputs are single-ended through SMA or differential through SMP connectors.

Clocking
The *d*HRFT is provided with an onboard sampling oscillator. If preferred an external clock source can be chosen.

FPGA
The Xilinx Virtex-6 FPGA is primarily dedicated to streaming baseband processing, also providing interfaces to ADCs and DACs.

Data Communication
Two GbE (optical/copper via SFP), serial port connectivity (RS232/USB) and PCIe up to x8 Gen 2 (adapter board).

Digital High Speed Connector
Connector for interconnecting of two or more *d*HRFT boards.

BSP (Board Support Package)
Adarate provides a BSP that implements the framework needed to build a complete data-transceiver-system.

Flexible analog front-end interface
The board can be equipped with a high quality single-ended or differential front-end with eg automatic gain-control to adjust to the input range of the ADCs.

Applications

- Broadband Communication Systems
- Radar Systems (Electronic Warfare)
- Protection Systems (ie DRFM/IED)
- Signal Processing (ie FFT)
- RF Down Conversion & RF signal generation
- Arbitrary Waveform Generation (AWG)
- Direct Digital Synthesis (DDS)
- Test Instrumentation